

of available link widths", where the multiplexer circuit is set to output the frame data according to a "selected active link width" specified in a received link management packet. McConnell et al. fails to provide any disclosure or suggestion of the claimed multiplexer circuit, as specified in independent claims 1 and 6. In fact, McConnell et al. only discloses multiplexers 1430 and 1450 which have nothing to do with switching between *a prescribed maximum link width* and a *selected active link width*, as claimed. The Examiner contends that McConnell et al. discloses that "the end node's port performs multiplexing means for combining packets of VL 0-15 as shown in fig. 6." Again, this is not a teaching of a multiplexer configured for switching between a prescribed maximum link width and a selected active link width, as claimed. In fact, no multiplexer circuit is shown in Fig. 6 of McConnell et al.

Further, the broadest reasonable interpretation of the claimed "link width" cannot be so broadly construed as to encompass *virtual lanes* (VLs), because such an interpretation would be inconsistent with the specification.

The specification explicitly distinguishes between virtual lanes and link widths: the specification describes that virtual lanes are serviced by a virtual lane arbitration module 64 (see Fig. 2) which determines "which virtual lane to service, in what order, and for what duration" (page 5, lines 20-24); in contrast, the specification describes that the multiplexer 76 of Figs. 2 and 3 is used to select a *link width* for transmission of the frame data (supplied at *the maximum link width*) to a physical network link that is connected to the channel adapter port.

Thus, the specification explicitly distinguishes between virtual lanes and link widths by specifying that the link width refers to the width of the actual width of the physical interface link (see also page 4, lines 4-11).

Hence, interpreting the claimed "link widths" as reading on virtual lanes would be

inconsistent with the specification and therefore unreasonable.¹

Further, the rejection fails to demonstrate that the applied reference inherently requires use of a multiplexer.² In fact, numerous variations may be implemented for responding to a link management packet, including implementing multiple link transceivers having respective data rates, where only one of the link transceivers is selected based on the corresponding link width specified in the received link management packet; hence, if a link management packet specifies a "4x" link width, one possible implementation would be for the channel adapter to enable the "4x" transceiver and disable the remaining transceivers (e.g., the "1x" transceiver and the "12x" transceiver). See, for example, column 14, lines 10-16 of McConnell et al.

In contrast, each of the independent claims specify the multiplexer circuit configured for “selectively switching frame data of a prescribed maximum link width”. As described in the specification, the “switching” in the multiplexer of Figure 3 includes not only transfer of data, but transfer of the data according to the appropriate width, and the appropriate sequence for transmissions using link widths smaller than the prescribed maximum link width:

The switch 96 is configured for switching the frame data according to the selected

¹“During patent examination, the pending claims must be ‘given their broadest reasonable interpretation consistent with the specification.’” MPEP §2111 at 2100-46 (Rev. 3, Aug. 2005) (*quoting In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)).

“The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach.” MPEP §2111.01 at 2100-47 (Rev. 3, Aug. 2005) (*citing In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)).

²See MPEP 2112 (“The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)(reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); ... ‘The mere fact that a certain thing may result from a given set of circumstances is not sufficient.’” (quoting *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999))).

Response filed March 2, 2007

Appln. No. 10/083,149

Page 3

active link width specified in the link width active register 18b based on the switching control signal 106 from the bus controller 62. Hence, the multiplexer circuit 76 may output *twelve (12) hyperbytes in sequence* for a 1x link, or *three (3) 4-hyperbyte groups in sequence* for a 4x link. In the case of a 12x link that corresponds to the prescribed maximum link width, the switch 96 selects a 108-bit bypass bus 110 that bypasses the multiplexer circuitry.

(Page 7, lines 1-6).

Still further, the Examiner contends that McConnell et al. discloses in Fig. 6 “outputting the frame data from the multiplexer circuit to a transmit bus according to the selected active link.” However, Fig. 6 of McConnell et al. does not disclose a multiplexer circuit or a transmit bus as claimed.

With regard to claims 2 and 7, there is simply no teaching in McConnell et al. of first and second multiplexer circuits as claimed. The Examiner mentions “multiplexing means (circuit)” of Fig. 6 of McConnell et al. but cannot identify such circuits by item numbers since no such circuits are shown or described in McConnell et al. Therefore, the rejection is improper and should be withdrawn.

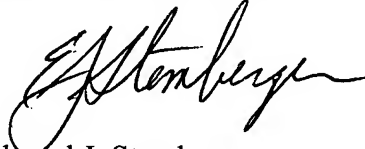
Hence, the rejection of claims 1 and 6, and the claims that depend there-from, should be withdrawn because it fails to demonstrate that the applied reference discloses each and every element of the claim. See MPEP 2131. “The identical invention must be shown in as complete detail as is contained in the ... claim.” *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). “Anticipation cannot be predicated on teachings in the reference which are vague or based on conjecture.” *Studiengesellschaft Kohle mbH v. Dart Industries, Inc.*, 549 F. Supp. 716, 216 USPQ 381 (D. Del. 1982), *aff’d*, 726 F.2d 724, 220 USPQ 841 (Fed. Cir. 1984).

In view of the above, it is believed this application is in condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-520, and please credit any excess fees to such deposit account.

Respectfully submitted,

Manelli Denison & Selter, PLLC

A handwritten signature in black ink, appearing to read 'E. Stemberger', written in a cursive style.

Edward J. Stemberger
Registration No. 36,017

Customer No. 20736
(202) 261-1014
Date: March 2, 2007